Asic Design Engineer

ROBERT SMITH

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Objective

As an Asic Design Engineer, responsible for the development of FPGA/ASIC devices. The individual will take a lead role in developing leading-edge digital imaging products for a pre-IPO company.

Skills

Oscilloscopes, Function Generators, Multi-meters, Spectrometers.

Work Experience

Asic Design Engineer

ABC Corporation - 2013 – 2016

- Worked both as an individual contributor and as a project lead to perform ASIC and FPGA-based design.
- Mapped complex DSP and digital coding algorithms into synthesizable VHDL and Verilog.
- Performed synthesis using Synopsys, Primetime, Synplicity, Xilinx ISE, Altera Quartus design tools.
- Responsible for top-level Synopsys synthesis scripts, as well as and sub-module scripts.
- Performed simulation using, ModelSim, Aldec, Cadence, and a variety of other simulators.
- Prototyped ASICs on Xilinx, Altera, and Actel FPGAs.
- Verified and validated all designs.

Asic Design Engineer

Delta Corporation - 2012 – 2013

- ASIC design is applied to data networking products involving both packets and SONET.
- Designed microchip devices used in fax, highlight color, and high-speed black and white printing products Coded, integrated, and simulated behavior.
- Defined and wrote chip specifications for the system, providing schedule planning, resource and tools requirements, and weekly interaction with the east.
- Provided schedule planning, resource requirements, and weekly interaction with team members, customers, and senior management in Webster, NY.
- Used Cadence Encounter APR tool for floorplanning, macro placement, gate sizing, region constraints of standard cell modules, congestion, and spacing.
- Currently working on RTL analysis of 224 bit Carry Propagate Adder in Xilinx- Vivado Developed test cases and test bench of three sub adders.
- Design of Ethernet switch ASIC chips using Verilog XL and synthesis using Synopsys.

Education

MS

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