



CHARLOTTE HARRIS

Senior Digital Design Engineer

✉ support@qwikresume.com

☎ (123) 456 7899

📍 Los Angeles

🌐 www.qwikresume.com

SKILLS

Strong Communication Skills



Project Management



Software Development



C/c++ Programming



Python Scripting



Matlab Prototyping



INTERESTS

📖 Birdwatching 🏠 Traveling

🏋️ Sports Coaching 🧶 Knitting

STRENGTHS

🔧 Pragmatism 🍃 Sensitivity

💖 Sincerity 📍 Stability

LANGUAGES



English



Mandarin



Swahili

ACHIEVEMENTS

🌟 Led the design and implementation of a high-performance FPGA-based system, resulting in a 30% increase in processing speed.

🌟 Developed a novel VHDL architecture that reduced power consumption by 25% in integrated circuits.

PROFESSIONAL SUMMARY

Accomplished Senior Digital Design Engineer with 7 years of extensive experience in crafting and optimizing advanced digital systems. Highly skilled in VHDL, RTL design, and FPGA implementation, I excel in enhancing performance and reliability of integrated circuits. Dedicated to utilizing innovative technologies to drive project success and deliver superior design solutions.

WORK EXPERIENCE

Senior Digital Design Engineer

📅 Mar / 2020-Ongoing

Quantum Solutions LLC

📍 Phoenix, AZ

1. Designed and optimized high-performance digital systems using VHDL and Verilog.
2. Conducted comprehensive system-level verification to ensure reliability and functionality.
3. Collaborated with cross-functional teams to integrate innovative design solutions.
4. Developed and maintained detailed documentation for design processes and methodologies.
5. Utilized FPGA technologies to enhance design capabilities and performance metrics.
6. Implemented design improvements that resulted in significant cost savings and efficiency gains.
7. Mentored junior engineers in best practices for digital design and verification.

Digital Design Engineer

📅 Mar / 2018-Mar / 2020

Cactus Creek Solutions

📍 Phoenix, AZ

1. Designed Xilinx and Actel FPGAs and CPLDs for advanced logging tools.
2. Engineered custom transmitter/receiver designs utilizing Manchester and NRZ encoding.
3. Created an Automatic Gain Control (AGC) unit to optimize input signal levels.
4. Developed a data logger for real-time display on logging systems.
5. Implemented designs on Xilinx Virtex-4 FPGA using VHDL and Verilog.
6. Debugged and enhanced depth/LAN logging boards for improved communication systems.

EDUCATION

Master of Science in Electrical Engineering

📅 Mar / 2016-Mar / 2018

Stanford University

📍 Toronto, ON

Focused on digital design and embedded systems.