

# **AVA DAVIS**

Failure Analysis Engineer

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#### PROFESSIONAL SUMMARY

Detail-oriented Failure Analysis Engineer with 5 years of experience in root cause analysis, semiconductor technology, and reliability testing. Proven track record in identifying failures and implementing solutions to enhance product quality.

## WORK EXPERIENCE

## Jr. Failure Analysis Engineer

## Blue Sky Innovations

T Chicago, IL

- 1. Conducted root cause analysis for advanced CMOS technology failures, improving product reliability.
- 2. Led Physical Failure Analysis (PFA) on semiconductor units, identifying critical failure modes.
- 3. Utilized nano-probing techniques to analyze devices at the 28nm technology node.
- 4. Performed electrical fault isolation using SEM and optical microscopy to diagnose issues.
- 5. Collaborated with cross-functional teams to enhance quality assurance processes.
- 6. Evaluated next-generation failure analysis tools, contributing to procurement decisions.
- 7. Participated in knowledge-sharing sessions, advancing team expertise in semiconductor failure analysis.

## Failure Analysis Engineer

#### Silver Lake Enterprises

**耳** Seattle, WA

- 1. Executed reverse engineering and de-processing for mixed signal and RF products, enhancing debug capabilities.
- 2. Applied RIE and plasma de-layering techniques for effective failure analysis.
- 3. Utilized advanced analytical tools, including SEM and AFM, for detailed failure investigations.
- 4. Developed and optimized etch recipes for cross-sectional analysis of semiconductor devices.
- 5. Interfaced with design teams to address layout issues impacting product reliability.

# **SKILLS**

Data Analysis

**Root Cause Analysis** 

**Electrical Fault Isolation** 

Physical Failure Analysis

Nano-Probing Techniques

## **INTERESTS**

Gaming

Fashion

🗐 Film

Technology

## **STRENGTHS**

Enthusiasm

Fairness

Flexibility

Forward-thinkina

## **LANGUAGES**





English 80%

Hindi 80%

Indonesian 80%

## **EDUCATION**

# Master of Science in Electrical **Engineering**

Dec / Dec / 2017 2019

Stanford University

Toronto, ON

Focused on semiconductor technology and reliability engineering.

## **ACHIEVEMENTS**

Reduced failure analysis turnaround time by 30% through process optimization.

Identified root causes of failures in 28nm technology, improving yield by 15%.