ROBERT SMITH

Verification Engineer

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SUMMARY

Verification Engineer with over three years of experience in verifying complex designs of High-Speed Ethernet IP using System Verilog (UVM), Verilog, Perl, and Shell Scripting. Experienced in full verification flow which includes test and coverage plan creation, environment, block functional model and scoreboards creation, test and coverage implementation, and results tracking to delivering fully verified IP designs.

CORE COMPETENCIES

System Verilog, RTL Design Using Verilog, Simulation Tools: Mentor Graphics QuestaSim, Cadence Incisive, Cadence IMC, C++, Perl, Shell Scripting, Microprocessor Architecture, Image Processing.

PROFESSIONAL EXPERIENCE

Verification Engineer

ABC Corporation - January 2013 – 2021

Key Deliverables:

- Verified the MAC and Statistics blocks The MAC implements standard IEEE 802.3 clause 3 features involving frame packaging and processing.
- Verified the MACSEC block compliant with IEEE 802.1AE Created test and coverage plans along with implementation of tests and functional coverage.
- Verified the Receive classifier that would preprocess the frames and extract useful information that would be used by the GCM-AES core.
- Designed, verified, performed RTL lint analysis and synthesis of MDIO Master and Slave, compliant with Clause 22 and 45 of IEEE 802.3 Ethernet standard.
- Bug analysis tool for mining data from Bugzilla using Perl scripting This was used in gathering important statistics related to bugs status which helped in methodology improvement.
- Verified BPAN compliant with Clause 73 of IEEE 802.3 standard.
- Created test and coverage plans along with implementation of tests and functional coverage for verification of 32G and 16G fibre channel using 64b/66b transmission word format and 8G, 4G and 2G fibre channel 8b/10b transmission word format.

Verification Engineer

Delta Corporation - 2009 – 2013

Key Deliverables:

- Created variants for North and South America, modifying xml files from the main SW programs in Beijing, Copenhagen and Finland.
- Ensured the work was completed meeting the customers demands and needs, by working with the SW program lead and the Project Manager assigned to the .

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- Hand tested samples to ensure that the product meet the customer requirements.
- Once approval was met, tested samples in a simulated factory environment to ensure quality.
- APS9800 - Hamilton Sundstrand, USA Tool Qualification of RTRT 2002, Diab 4.4b and Single Step Simulator 7.6.6 environment.
- Designed test cases, scripts to achieved results for all the C constructs.
- CFC A380 and APS9800 - Hamilton Sundstrand, USA Verification activity on a Condenser Fan Controller.

EDUCATION

Master of Science

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